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1 A Programmable Boundary Scan Technique for Board-level, Parallel Functional Duplex March Testing of Word-Oriented Multiport Static RAMs

Kanad Chakraborty, Pinaki Mazumder

March 1997 **Proceedings of the 1997 European conference on Design and Test**

Full text available: pdf(592.85 KB) Publisher Site

Additional Information: full citation, abstract

A framework for integrating boundary scan (IEEE 1149.1) with board-level self-testing of word-oriented, multiport static RAM chips is proposed. Innovative parallel versions of functional duplex march tests (FDMs) for detecting complex couplings are developed. This approach produces significantly smaller cycle-time penalty during normal operation than built-in self-testing (BIST). It produces two orders of magnitude test acceleration as compared to pure boundary scan testing without BIST (i.e., b ...

Keywords: Boundary scan, bus interface unit, march tests, functional duplex march algorithms (FDM)

2 New test methods targeting non-classical faults: Embedded software-based self-testing for SoC design

A. Krstic, W. C. Lai, K. T. Cheng, L. Chen, S. Dey

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(324.94 KB) Additional Information: full citation, abstract, references, index terms

At-speed testing of high-speed circuits is becoming increasingly difficult with external testers due to the growing gap between design and tester performance, growing cost of high-performance testers and increasing yield loss caused by inherent tester inaccuracy. Therefore, empowering the chip to test itself seems like a natural solution. Hardware-based self-testing techniques have limitations due to performance and area overhead and problems caused by the application of non-functional patterns. ...

Keywords: SoC test, VLSI test, functional test, microprocessor test

3 Microprocessor based testing for core-based system on chip

C. A. Papachristou, F. Martin, M. Nourani

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(832.80 KB) Additional Information: full citation, references, citings, index terms

4 Embedded hardware and software self-testing methodologies for processor cores

Li Chen, Sujit Dey, Pablo Sanchez, Krishna Sekar, Ying Cheng